10µm Radiation Tolerant Global Shutter Pixel for Operation under High Ionizing Dose Rates of Gamma or X-ray Radiation

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***Abstract* — A 10x10 µm² radiation-tolerant voltage domain global shutter pixel with radiation hardened by design (RHBD) devices modification is developed to operate under high ionizing dose rates and high total ionizing dose (TID) levels. Therefore, a modified NMOS transistor layout is used in the pixel to achieve radiation hardness. The pixel design is demonstrated to operate up to 1MGy, 100Mrad (SiO_2) TID, with minimal degradation. The global shutter pixel also includes correlated double sampling (CDS) to reduce noise and collected carriers generated by the flux of gamma or x-ray radiation. Combined with an external flash, global shutter operation allows short exposures, which limits the impact of radiation on dark current and dynamic range. The pixel is designed using 180nm CMOS Image Sensor (CIS) technology.**

Keywords — CMOS Image Sensors, Total Ionizing Dose (TID), Global Shutter, Xray.

I. INTRODUCTION

Nowadays, CMOS Image Sensors (CIS) are required in various applications: from consumer, industrial, medical and scientific. For special applications such as ionizing radiation environments, CIS are the most promising type of photodetectors for performance imaging applications where radiation hardening is required: space, nuclear, scientific, medical or even military operations. Multiple solutions have been proposed in the last years with rolling shutter 3T or 4T pixel architectures [1]. However, rolling shutter operation presents some limitations, like acquisition speed, motion artifacts or synchronisation.

Global shutter pixels also support flash illumination with short exposure time [2], which compensates the contribution of directly generated carriers from gamma or x-ray radiation through Compton scattering or the photoelectric effect [3] to the photosignal. The result is a lower noise operation with short exposure and limited degradation with TID.

A. Radiation Effects in Electronics

Electronic devices and, therefore, CMOS transistors are impacted by ionizing radiation through the cumulative creation of positive charges in the SiO_2 dielectric layers and an increase of interface states at the Si-SiO_2 interface. These lead to a shift of threshold voltage (V_{th}), a degradation of the carrier's mobility - µ the increase of 1/f noise and the formation of a parasitic source-drain leakage path via the STI and field in the n-MOSFET.

In CMOS pixels, these effects lead to an output offset and a 1/f noise increase, lateral shunting between pixels, lower gain and increase of the photon response non-uniformity (PRNU), and an increase of the average dark current (I_{dark}) and, therefore, dark signal non-uniformity (DSNU). The I_{dark} increase, especially at low TID levels, is dependent on the presence of sidewall trench isolation (STI) along the channel and due to the increase in interface state density combined with the depletion region modification close to the surface [4]. To limit the impact of TID effects, new device layouts were studied. V_{th} shift, 1/f noise and µ cannot be improved just by design since they rely on technology parameters: the thickness of SiO_2, the W/L of the transistor and the doping concentrations. Therefore, the focus is on minimizing the source to drain leakage which significantly impacts the pixel performance. Using the enclosed layout transistor (ELT) [4] [5], there is no STI along the channel, and the connection between the drain and the source cannot be built. ELT devices, however, require more area compared to straight devices. Being fully enclosed, the gate is significantly larger and therefore, the W/L ratio is larger than the smallest straight devices in the same technology. Additionally, the outer terminal, typically the drain in n-MOSFET, is unshielded and requires a guard ring to avoid leakage to neighbour transistors. All this requires space, which is critical in pixel design, especially for small pixel pitch design.

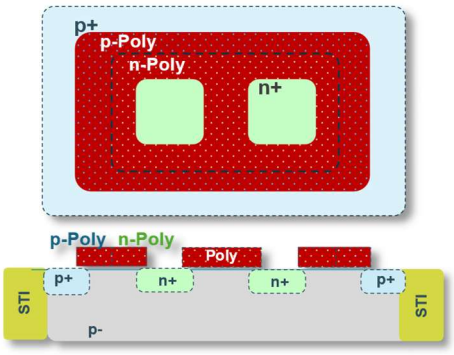

Fig. 1. Butterfly (BF) NMOS Device, a compact enclosed device.

An alternative to ELT devices as enclosed devices is the butterfly (BF) MOSFET (Fig. 1) [4], which is a fully enclosed device with a compact layout scheme and a small W/L ratio. Since both drain and source are fully enclosed with a polysilicon gate, no lateral STI is present and, thus, no formation of leakage paths up to high TID levels. To increase the radiation tolerance for very high TID, a p+ implant is deposited from the outer half side of the polysilicon gate enclosure.

For 180nm CMOS and higher than 1MGy TID (SiO_2), CMOS devices V_{th} shifts are of +0.15V in NMOS and -1.0V in PMOS, respectively, and have been measured in the selected process. In addition, up to 40% mobility degradation is expected on devices with a length below 0.44 µm [4] [5].

For this reason, no minimal-size transistor was used in the work.

II. Global Shutter Pixel with RHBD Devices

The pixel is designed with "butterfly" NMOS transistors (BF), eliminating parasitic field leakage currents by design. As discussed, for pixel arrays, the most critical aspect is area, and the pixel electronics are expected to be as small as possible to guarantee the maximum fill factor. The BF transistor is a fully enclosed device with a compact layout scheme and a small W/L ratio.

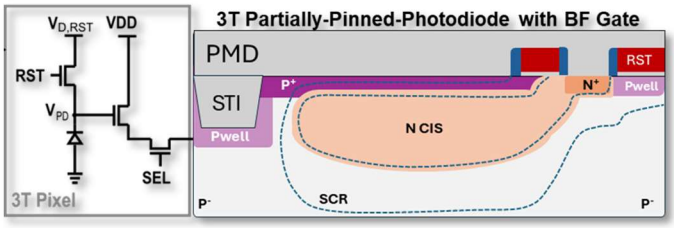

Fig. 2. A 3T Pixel configuration for Radiation conditions.

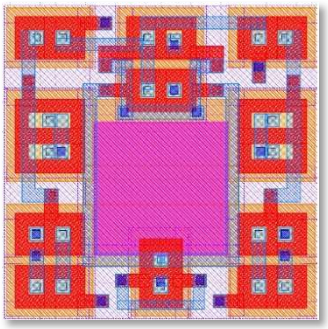

Fig. 3. Global shutter layout proposal.

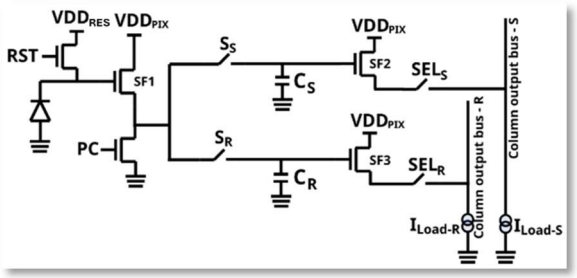

Fig. 4. Schematic of the global shutter pixel.

The Pixel architecture (Fig. 3 and Fig. 4) has 9 transistors and 2 capacitive storage nodes. All the devices are BF-type devices, including the storage nodes. The pixel is tested up to 1MGy (100Mrad) TID (SiO_2) with X-ray radiation. To withstand such a high TID value, a partially pinned photodiode is used (Fig. *2*) [6]. The intentional use of a strong p+ implant on the photodiode and recessed shallow trench isolation (STI) reduces the dark current from the TID-induced interface traps and SiO_2 interface while also shielding the photodiode region from TID-induced positive charges in the SiO_2. In-pixel storage nodes or memories are implemented by MOS capacitors, which are also inherently radiation tolerant.

The PD connects the n^- implant to the gate of the source follower (SF1) and the drain of the reset switch. To read the SF1 voltage, an active load or precharge (PC) is used. The pixel reset voltage – when PD is being reset – and pixel signal voltage – at the end of the PD exposure – are stored in two storage nodes: the CS and CR MOS capacitors. For these, dedicated switches (SS and SR) are used to connect to two independent output buses. The proposed pixel architecture does not use a transfer gate (TG) Fig. *2*. For very high TID (> 10 kGy TID), the transfer gate degrades with TID due to a significant charge transfer efficiency (CTE) drop and lag increase, caused by a drop in carrier mobility μ and charges built-up in oxide and spacer regions [6] [7] [8]. For the same reasons, a charge domain global shutter architecture was not considered.

The pixel is designed using 180nm CMOS Image Sensor (CIS) technology. Currently, X-ray radiation is used for TID accumulation. Future Co^{60} experiments are considered for radiation degradation investigation purposes.

III. Experimental Results

Testchips with the presented GS pixel architecture were evaluated before and after irradiation. The results and the respective discussion are presented in this section. The testchip includes a small matrix of 8 x 8 pixels. The applied timing is presented in Fig. *5*, and the supply levels are VDD_{RES} = 2.8V and VDD_{PIX} = 3.3V. The testchips have independent analogue outputs for pixel signal and pixel reset values (Fig. *4*). The acquisition system used a dual 14-bit resolution ADC that acquired the pixel signal and pixel reset simultaneously. The conversion step of the ADC is 152.7 μV/DN. For all testchips and all measurement conditions the PD is operated in hard reset to avoid low illumination non-uniformities.

Fig. 5. Timing scheme of the global shutter pixel.

There were also 2 process split lots available for comparison. The original split includes all the standard CIS process doping, while in the second split lot, the photodiode implant is less abrupt, which can reduce the dark current after radiation. In this article, the original split is named OR, and a second split lot is named the SP. The individual device name convention is ORxx and SPxx, where xx is the device number.

Testchips were measured before and after radiation steps in multiple setups and temperature conditions. The X-ray equipment is an XRD diffraction tube with tungsten target material that produces high-energetic photons with peak spectrum at 10 keV. The produced dose rate for this experiment was 3.6 kGy/h (100 rad/s) for the entire radiation campaign.

There are 2 radiated testchips up to 1MGy TID (SiO_2), where during HTA, the sample SP02 was kept unbiased, while sample SP03 was kept biased. For the SP split, the highest TID level is 1MGy TID (SiO_2) followed by a high-temperature annealing (HTA). The HTA consist of keeping the device at a constant temperature of 100ºC for 7 days (168h). The OR split was radiated just until 580kGy and followed by an annealing step as described.

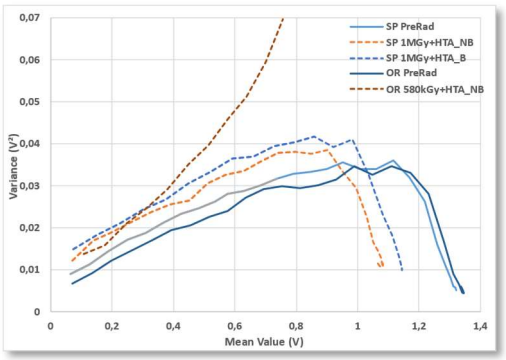

Fig. 6. PTC curves comparison of OR and SP splits, before and after high TID levels (SiO_2).

The PTC curves (Fig. *6*) show the signal-noise relation with the split lot and the TID levels. The biggest impact of radiation is observed on the split lot. Regardless of the BF transistor implementation in pixel, the photodiode implant doping with higher concentration (OR split) generates a significant dark current after radiation. This is due to higher doping resulting in an abrupt n+/p+ junction and therefore higher dark signal with TID. OR split already shows a large degradation at half of the target TID level (580kGy). The SP split, on the other hand, has a marginal impact after 1MGy TID (SiO_2). Additionally, the peak point of PTC after radiation and for SP split shows a reduction of around 20%. This is not due to FWC reduction on the photodiode, which remains constant, but due to an output swing reduction caused by the transistor's V_{th} shift.

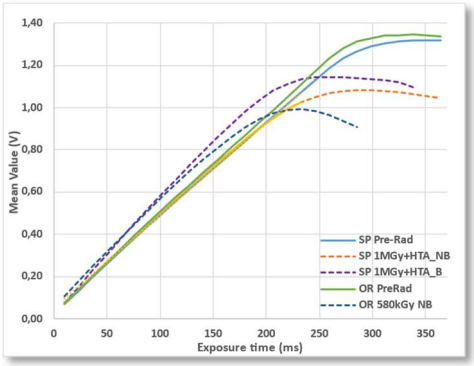

Fig. 7. Response curves comparison of OR and SP splits, before and after high TID levels (SiO_2).

The response curves (Fig. *7*), are in line with PTC. SP lot shows almost no degradation, except for the output swing reduction. This fact is due to radiation effects on CMOS devices where the V_{th} shifts, limiting the working range of the pixel itself. This is true for pixel source followers and for the testchip readout circuit where both NMOS and PMOS transistor-based circuits are present and where TID effects limit the operational voltage swing.

The dark current evolution with temperature and radiation is presented in Fig. 8. On the left side, the evolution of dark current with temperature is shown before and after Radiation. With the increase of TID the depletion region changes close to the surface, increasing the dark current. Combined with interface state density the variation of the dark current with temperature is significantly modified. The increase in TID is due to the change in the depletion region, the excess of collected charges and the increase in interface surface density.

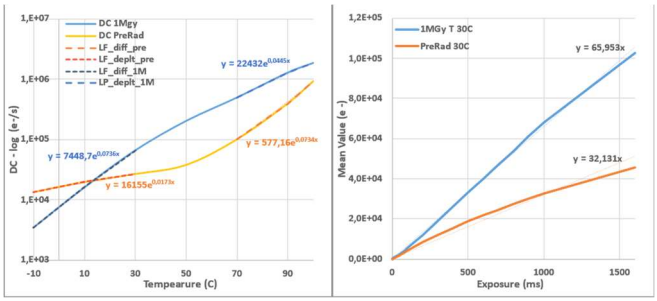

Fig. 8. Dark current figures of the SP split before and after radiation with Temperature (left) and with exposure time (right).

On the right side, the dark current evolution with the exposure time is shown at a constant temperature of 30C. It is possible to observe that the TID doubles the I_{dark} compared to the pre-radiation condition. The signal is reasonably linear.

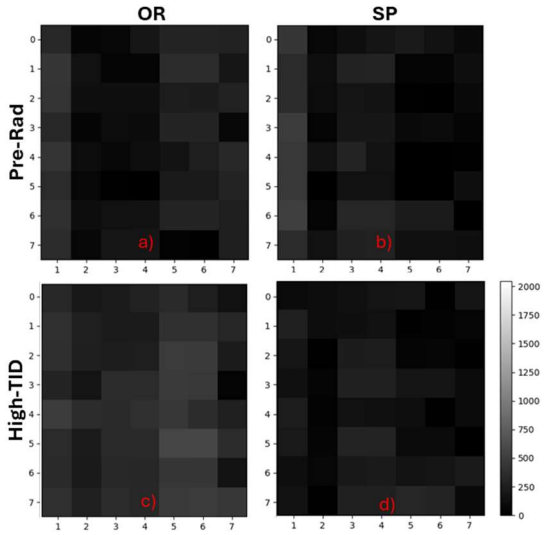

Fig. 9. OR and SP split dark images with 10ms exposure and 8x gain. a) OR split pre-rad; b) SP split pre-rad; c) OR split 580kGy TID (SiO2); SP split 1MGy TID (SiO2).

Fig. 9 presents images in dark conditions from OR (left side) and SP (right side) splits before and after the radiation campaign with a gain of 8x and 10ms exposure time. The right-side scale presents values in DN. The non-radiated condition shows similar results and noticeable column FPN. The presence of a relatively strong column FPN is due to the readout columns being a radiation-hardened design without a common reference signal or offset compensation, resulting in a considerably strong column FPN mainly due to device mismatch. This FPN is expected to increase with TID due to transistor mismatch increase. The images from the irradiated devices c) and d) have some visible degradation; in particular, the OR split (left) after 580kGy TID (SiO_2), which shows a more noticeable degradation of the pixel response.

In Fig. 9 it is also possible to observe a strong DSNU, besides the column FPN. With TID increase multiple mechanisms take place: 1 - the radiation-induced defects have a non-homogeneous distribution across the pixel, enhancing the dark current non-uniformity (DCNU) 2 – the pixel devices mismatch increases leading to a greater signal non-uniformity when compared with before radiation.

Table *1*. presents a numerical compilation of the measured parameters of the measured devices. The conversion step of the ADC is 152.7 µV/DN. The first important fact is that for

this particular demonstrator, the CDS cannot completely eliminate the read noise and therefore it is considerably high before radiation.

Param.	*OR Pre-rad*	*OR 580kGy*	*SP Pre-rad*	*SP 1MGy + HTA NBias*	*SP 1MGy + HTA Bias*	*Units*
Read noise	164.4	360	139.8	200.2	255.4	e^-_{RMS}
Conversion gain	5.30	10.49	5.96	5.64	5.89	uV/e-
FWC	198001	90023	172049	176245	175980	e-
Dynamic Range	61.61	57.3	61.80	58.7	57.69	dB
DSNU	361	429	297	303	311	e-
PLS	0.0046 (1:22000)	0.052 (1:1950)	0.0023 (1:43000)	0.014 (1:7400)	0.009 (1:11300)	%

Table 1. Summary of pixel parameters with TID and splits

There are two reasons to explain this. First, the pixel is based on a 3T architecture, and thus, the PD cap results in a greater kTC and 1/f noise resulting in a large read noise. This capacitance is estimated to be C_{PD} ≈16.6 fF, including parasitics, leading to a kTC noise of 74 e^-_{RMS}; 2. The storage capacitance C_{SS} = C_{SR} is estimated to be 21 fF each, or just slightly larger than the C_{PD}, meaning that the individual kTC of the storage capacitance is also included in the generated signal. Thus, the resulting calculated read noise is around 146 e^-_{RMS}. Pixel temporal noise would be considerably reduced with larger storage capacitors, as can be offered by deep trench capacitors in modern CIS processes. However, comparing the read noise before and after TID, especially of the SP split, the increase is just marginal.

Given the TID values of the OR split, the degradation observed is too great by the test results and therefore will not be considered as a possible solution.

For the SP split lot, the conversion gain variation is also minimal from before to after radiation, this means that marginal gain variation is expected with the present architecture for this split. Additionally, for the SP split, the FWC is kept close to 175ke-, as expected.

The dynamic range reduction is due to the output swing reduction, mainly due to the V_{th} shift and mismatch increase of all transistors in the pixel and readout chain.

Another important parameter regarding the Global shutter pixels is the Parasitic Light Sensitivity of the storage nodes (PLS), defined as the ratio of sensitivity of the storage nodes over the sensitivity of the photodiode, after CDS. Both splits have a reasonable PLS before radiation (1/22000 or better), which drops to 1/7400 after 1 MGy and unbiased thermal anneal. The leakage current on the storage capacitors increases from 0.8mV/s pre-rad to 9.98 mV/s after 1MGy (SiO2). Most of this increase is cancelled after (correlated) double sampling since it is similar on both capacitors.

IV. Discussion

The 10x10 μm^2 voltage-domain global shutter pixel uses device-level modifications that effectively mitigate total ionizing dose (TID) effects and read noise increase by using correlated double sampling (CDS).

The use of BF device modification enabled the required radiation tolerance for the TID levels up to 1 Mgy (SiO2). The photodiode modifications: partially pinned, recessed STI and PD implant reduction, show an increase in robustness to TID and moderate I_{dark} increase.

The presented GS pixel SP split, utilizing a less abrupt photodiode junction, shows radiation tolerant to up to 1MGy TID (SiO_2) with marginal degradation.

The focus of this development is on high TID effects tolerance, therefore, the pre-radiation results are modest comparing the state-of-the-art, once the focus was to implement novel RHBD strategies that achieve the end goal, being conservative concerning pre-radiation noise performance.

Future designs should improve read noise and seek for improved photodiode architectures and true CDS operation resulting in a radiation hardness and low noise pixel architecture.

V. Acknowledgement

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VI. References

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